REMARKS

The Office Action of November 5, 2004 has been received and its contents carefully considered. An RCE is being filed to relieve the application of its finally-rejected status.

The present Amendment revises the claims as in the Amendment After Final Rejection that was filed on February 3, 2005, except (1) a comma that was accidentally missing from the revisions to claim 8 has been added, and (2) new dependent claims 9 and 10 are being added to further protect the invention.

The present Amendment revises claim 4 by correcting "date" to "data." It is respectfully submitted that this cures the antecedent basis problem identified in section 3 of the Office Action, so that the rejection for indefiniteness should be withdrawn.

The present Amendment also corrects an oversight in claim 8, by deleting a redundant "memory device" that was added by mistake in an earlier Amendment. In addition, the present Amendment revises claim 8 to specify that a switch between a test port and a CPU is selectively turned off if a stored security bit has been changed to a predetermined state.

Finally, the present Amendment adds two new dependent claims, as was noted above.

A common feature found in the various embodiments disclosed in the present application is that a control circuit is present to allow or disallow an exchange of signals between a JTAG (Joint Test Action Group) port and a TAP (Test Access Port). For this purpose, the control circuit uses a security bit that is stored in an electrically rewritable ROM. As the present application explains on the first page, the mere presence of the security bit in an electrically rewriteable ROM did not always protect the content of the ROM adequately in the past, if an unauthorized person used a JTAG port to directly insert a command to the CPU of the equipment having the ROM to read out the content of the ROM. The various embodiments disclosed in the

present application prevent an unauthorized person from circumventing the protection provided by a security bit by controlling signal exchange between a JTAG port and a TAP port in accordance with the state of the security bit. As a result, an unauthorized person cannot use a JTAG port to feed in an instruction for reading out the content of the ROM after the security bit has been set.

Section 5 of the Office Action rejects independent claims 1 and 8 for anticipation by patent 6,662,314 to Iwata et al. This reference will hereafter be called simply "Iwata." For the reasons discussed below, it is respectfully submitted that claims 1 and 8 are patentable over Iwata.

The Iwata reference is directed to an improved technique for debugging a microcomputer having an internal flash memory. Figure 1 of the reference (the same figure that is reproduced on the cover page of the patent) illustrates a microcomputer 1 having an internal flash memory 5 that includes a control circuit 5c. Iwata's control circuit 5c allows or disallows a write into Iwata's flash memory 5 on the basis of a flash protect signal and a mode signal that are received by an OR-gate 5b. It is noteworthy that neither Iwata's flash protect signal nor his mode signal is supplied to his debugging module 4, which is disposed between Iwata's debugging tool 2 and a bus in Iwata's microcomputer 1.

Independent claim 1 recites a JTAG port, a TAP, and a flash ROM which stores a security bit. Claim 1 concludes by reciting "a JTAG control circuit controlled by the security bit of the flash ROM, the JTAG control circuit being connected between the JTAG port and the TAP and allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit."

The Office Action takes the position that Iwata's component 15, which is shown in Figure 2 of the reference, corresponds to both the TAP of claim 1 and the JTAG control circuit of claim 1. Identifying both the TAP and the JTAG control circuit of claim 1 with the same component of the reference is problematic, since claim 1 provides that the JTAG control circuit is connected between the JTAG port and the TAP. How could Iwata's component 15 be connected between itself and Iwata's component 11? Similarly, how would it be possible for Iwata's component 15 to allow or prevent communication between itself and Iwata's component 11? It is respectfully submitted that the whole concept of allowing or preventing an exchange of signals within a single component is misplaced.

The Office Action relies, in part, on the passage at column 5 of Iwata, line 63, to column 6, line 3. However, this passage mainly states that Iwata's reference number 15 denotes a JTAG control unit that carries out communication with Iwata's debugging tool 2 via terminals 11, and that a TAP controller controls access from the terminals 11. This passage does not disclose or imply that an exchange of signals between a JTAG port and a TAP is allowed or disallowed using a security bit stored in an electrically rewriteable ROM. Accordingly, it is respectfully submitted that the invention defined by claim 1 is patentable over Iwata.

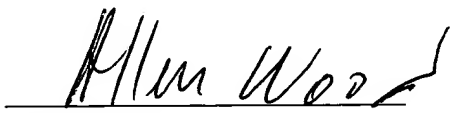
Turning now to independent claim 8, the "security releasing means" previously recited in the claim has been changed to a "security control means" that selectively turns a switch off if a security bit has been changed to a predetermined state, in addition to turning the switch on if two data agree (as previously recited). The Office Action refers to a passage at column 18 of the reference, line 66 to column 19, line 10. However, this passage only discloses that control is implemented so as to allow a data read based on the security level and a value input by a keyboard. There is no suggestion in the reference of a means "for selectively turning off the

switch if the security bit has been changed to a predetermined state" and for turning the switch on when two data disagree, in accordance with the present formulation of claim 8.

New claim 9 depends from claim 8 and is therefore patentable along with claim 8. It is nevertheless noted that claim 9 recites "a gate having an output terminal that is connected to the switch and having a plurality of input terminals, one of the input terminals receiving the security bit." This is neither disclosed nor suggested by Iwata. In particular, the output terminal of the gate 5b in Iwata's Figure 1 is connected to Iwata's memory, and the JTAG control unit 15 in Iwata's Figure 2 is not connected to Iwata's gate 5b.

For the foregoing reasons, it is respectfully submitted that the rejection of claims 1 and 8 for unpatentability over the prior art should be withdrawn, as should the rejection of claims 4-7 for indefiniteness. Accordingly, reconsideration of this application is respectfully requested.

Respectfully submitted,



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